Attorney Docket No.:ITEX-99001C2

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Application of: *Liu et. al.*	)	Art Unit: *unknown*
Serial No.:*unknown*	)	Examiner: *unknown*
Filed: 11/13/01 as a continuation of serial no. 09/255,235 filed 2/22/99	)	
For: *DSL Link with Embedded Control and Multi-Channel Capability*	)	

PRELIMINARY AMENDMENT

Commissioner of Patents and Trademarks
Washington, D.C. 20231

Sir:

Applicant respectfully submits the following amendment and response to place this case in condition for allowance:

IN THE SPECIFICATION:

Please change the title of the invention to read:

-- DSL Link with Embedded Control and Multi-Channel Capability --

Please substitute the following for the Abstract:

ABSTRACT OF THE DISCLOSURE

A digital communications link, protocol and related circuits are disclosed which use an embedded control channel for transferring control information between different sections of an xDSL system, including within a personal computer. The control channel is included as part of a data frame structure that is suited for a multi-channel communication system, including in an xDSL communications environment.

Please delete the text at page 5, lines 5 – 17 and enter the following as a clean version substitute for such paragraph:

An improved digital communications link of the present invention connects a digital controller section of an xDSL modem - which is preferably located on a system motherboard of a computing system - to a separate analog section of the xDSL modem - which is located at a position substantially free of electronic noise from other electronic components on said motherboard, which could materially affect the operation of such analog section. The data path/link is generally configured in the following manner: (a) a plurality of receive signal lines are set up for receiving data from a remote site; (b) a plurality of transmit signal lines are designated for transmitting data to a remote site; (c) a bit clock signal line is set up for carrying a clock signal, which clock signal is used in connection with communicating the data to and from the remote site. The bit clock signal line can carry any desired clock signal needed according to data transmission requirements of said digital communications link, thus providing a scalable interface that is easily adaptable for use in any number of different motherboard environments.

Please enter the following as a clean version substitute for the paragraph in the specification at page 10, lines 1 – 11:

216, which transmits signals in the DSL link to DSL Digital Modem Circuit 230, and converts received signals in the DSL link to various data and control signals for the internal circuits within DSL Analog Modem Circuit 205, including control registers 215. Also inside DSL-A 216 is a clock circuit (not shown) which generates the necessary clocks for internal blocks and external DSL link based on an input from a System Master Clock as shown. Again, some or all of the functions of DSL Analog Modem Circuit 205 may be grouped and implemented in single chip form. For example, DSL-A codec 218, incorporating control registers 215, DSL-A Interface 216, digital filters 214, 214', and A/D 213 and D/A 213' is preferably embodied in a single integrated circuit (IC), and a separate IC is preferably used to embody analog front end sections (i.e. receive/transmit drivers 209, 209' and receive/transmit filters 211 and 211').

Please enter the following as a clean version substitute for the paragraph in the specification at page 11, lines 27 – 29:

As noted above, functions performed by Transmitter Buffer and Processing 234' and Receiver Buffer and Processing 234 depend on the specific xDSL implementation. In the case of host signal processing, where the present invention can be used for great

Please enter the following as a clean version substitute for the paragraph in the specification at page 12, lines 24 – 26:

Receive data lines RX_1 - RX_4 carry digital samples generated by A/D 213 and assembled and transmitted across the link by DSL-A Interface 216; DSL-D interface 233, conversely dis-assembles and passes these samples on for further signal processing.

Please enter the following as a clean version substitute for the paragraph in the specification at page 18, lines 11 – 29:

--Reuse of DSL Link for External Hardware DSL Implementation

As mentioned earlier, the use of DSL Link 220 is most attractive to a host based DSL modem implementation requiring minimal logic inside Digital IC 230. When the CPU in the motherboard is not fast enough, it is desirable to use the DSL Link to connect Digital IC 230 to an external hardware DSL implementation. In this case, another useful aspect of the present invention is illustrated in FIG. 4. As shown, when an external hardware solution for a DSL modem implementation exists, a reasonable interface to use with such implementation is one based on the ATM Utopia I or Utopia II interface. This is because ADSL technology has already been defined to interface with ATM in both T1.413 Issue 2 and ITU-T G.992 standards. In this configuration, DSL Digital IC 230 would be linked through DSL Digital Link 220 to a hardware based xDSL modem in FIG. 2A and 2B, instead of interfacing directly to DSL Analog Modem Circuit 205. In such instance, of course, since most of the signal processing and control functions would be located within the hardware xDSL modem, DSL Digital Controller 230 could be simplified accordingly. The reason this is possible is because the same 10 signal lines described above (RX_1 - RX_4, TX_1 - TX_4, CLOCK and WORD CLOCK) can serve a dual purpose and act as an ATM interface as well. As above, for the same four sampling cycles per word clock, the following data can be transported over DSL digital link 220:

1. First clock cycle period: RX_1 - RX_4 are used for Control, 0, RxClav, TxClav;

Please enter the following as a clean version substitute for the paragraph in the specification at page 19, lines 1 – 7:

TX_1 - TX_4 are used for Control, 0, RxEnb and TxEnb.

2. Second clock cycle period: RX_1 - RX_4 are used for RxSoc, RxAddr [2:0], while TX_1 - TX_4 are used for TxSoc, TxAddr [2:0].
3. Third clock cycle period: RX_1 - RX_4 are used for RxData [7:4], while TX_1 - TX_4 are used for TxData [7:4].
4. Fourth clock cycle period: RX_1 - RX_4 are used for RxData [3:0], while TX_1 - TX_4 are used for TxData [3:0].

IN THE CLAIMS:

Please cancel claims 1 – 16, 22 – 26, 32 – 36, and 42 - 60.

Please substitute the following as a clean set for remaining claims (17 – 21, 27 – 31, 37 – 41, 61 - 66:

17. (Amended) A method for transmitting data on an xDSL digital communications link between a digital controller and an analog codec located within a personal computer system, the method comprising the steps of:

(a) generating a bit clock adapted for data transmission requirements of the xDSL digital communications link;

(b) communicating the data and operational and/or control information between the digital controller and analog codec at a rate corresponding to said bit clock such that said operational and/or control information is transmitted over a data line during a first time period corresponding to a first number of bit clock periods, and the data is transmitted over said data line during a second time corresponding to a second number of bit block periods;

wherein both said operational and/or control information and the data can be exchanged between the digital controller and the analog codec over a time division multiplexed data line.

18. (Amended) The method of claim 17, wherein said operational and/or control information includes information relating to real time control settings for circuits located within the analog codec.

19. (Amended) The method of claim 18, wherein said operational and/or control information further includes information relating to power management for an xDSL modem.

20. (Amended) The method of claim 19, wherein said operational and/or control information consists of control data words that are transmitted asynchronously with respect to the data.

21. (Amended) The method of claim 20, wherein said operational and/or control information consists of a control data word, and wherein a start bit is used within said operational control information to indicate the beginning of a valid control data word.

27. (Amended) A method of operating a multi-channel digital communications link within a personal computer system, the method comprising the steps of:

(a) generating a bit clock signal and a separate frame signal adapted for data transmission requirements of a plurality of separate communications channels within the personal computer system;

wherein said plurality of separate communications channels are supported by a communications bus coupling a digital controller and a plurality of separate communications circuits within the personal computer system;

(b) communicating data words between said digital controller and one or more of said plurality of separate communications circuits using said bit clock signal and said separate frame signal;

(c) grouping data words for one or more of said separate communications channels in a multi-channel data frame such that each of said plurality of separate communications circuits can be supported with a different transmit and/or receive data rate over said communications bus.

28. (Amended) The method of claim 27, wherein said frame signal is used to mark the boundary of each multi-channel data frame by having a first predetermined value for a first number of bit clock cycles at the frame beginning, and said frame signal has a second predetermined value for the rest of said multi-channel data frame.

29. (Amended) The method of claim 27, wherein operational and/or control information for each of said plurality of separate communications circuits is embedded in data words communicated through each of their respective communications channels.

30. (Amended) The method of claim 29, wherein said operational and/or control information consists of control data words that are transmitted asynchronously with respect to data words.

31. (Amended) The method of claim 27, wherein the digital controller section is located on a system motherboard of the computing system, and the separate communications circuits include at least one with an analog codec located at a position which is substantially free of electronic noise from other electronic components on said motherboard which could materially affect the operation of such analog codec.

37. (Amended) A digital controller for use with an xDSL compatible modem comprising:

a) means for processing xDSL formatted data in accordance with an xDSL transmission protocol; and

b) means for generating control signals associated with maintaining an xDSL compatible data link within a computer system in accordance with said xDSL transmission protocol; and

c) a digital interface for coupling the digital controller to an analog codec associated with the xDSL compatible modem and, said digital interface being configured such that:

[i] a plurality of receive lines can be used for receiving xDSL data; and

[ii] a plurality of transmit lines can be used for transmitting xDSL data;

[iii] a bit clock signal line can be used for carrying a bit clock signal adapted for said xDSL transmission protocol; and

[iv] a frame signal can be used for clocking xDSL data in the form of an xDSL data frame transferred in parallel over said plurality of receive lines and/or said plurality of transmit lines; and

[v] a control channel is provided so that said control signals can be passed between said digital controller and said analog codec sections of said xDSL capable modem within at least one bit clock signal period of one or more of said xDSL data frames using said plurality of receiving lines and/or said plurality of transmitting lines; and

wherein said digital controller is adapted to be physically placed on a computer motherboard.

38. (Amended) The digital controller of claim 37, wherein said control signals are embedded within an xDSL data word and asynchronously transmitted with respect to xDSL data words contained in said xDSL data frames.

39. (Amended) The digital controller of claim 37, wherein said digital interface can handle a multi-channel xDSL data frame, said multi-channel xDSL data frame having at least two data channels, and wherein data can be transferred through a first channel during a first time period of said multi-channel xDSL data frame, and through a second channel during a second time period of said multi-channel xDSL data frame.

40. (Original) The digital controller of claim 37, wherein said control signals relate to real time control settings for circuits located within the analog codec.

41. (Amended) The digital controller of claim 37, wherein said control signals relate to power management operations to be performed by the xDSL capable modem.

61. (Amended) In a motherboard for use in a personal computing system, and which system is configured to support a plurality of separate communications channels using a multiplexed communication bus within the personal computing system, the improvement comprising:

(A) a digital controller controlling data transfers over the multiplexed bus, said digital controller being located physically on the motherboard and including:

[i] circuitry for processing data and control signals for each of the plurality of separate communications channels; and

(B) an analog front end circuit associated with a first one of said plurality of separate communication channels, said analog front end circuit being electrically coupled to the multiplexed bus but physically separated from said digital controller, said analog front end circuit including:

[i] line interface circuitry for coupling to a first data channel carrying analog data signals corresponding to first data transferred in accordance with a first communications standard and control signals associated with a first data transmission; and

[ii] circuitry for performing A/D and D/A operations on said analog data signals and first data signals respectively; and

(C) a digital interface for coupling said digital controller and analog front end circuit over the multiplexed bus, said digital interface including:

[i] a plurality of data receiving lines; and

[ii]a plurality of data transmitting lines; and

[iii] a clock signal adapted for supporting transmission requirements of each of said plurality of separate communications channels; and

wherein a plurality of separate control channels are implemented in time-multiplexed form over the multiplexed bus for each of said plurality of separate communications channels respectively.

62. (Amended) The motherboard of claim 61, wherein said analog front end circuit is located on a xDSL modem riser card which is configured to be mounted substantially perpendicular to the motherboard.

63. (Original) The motherboard of claim 61, wherein said digital controller is controlled in part in software by a host processor located on the motherboard.

64. (Amended) The motherboard of claim 61, further wherein said digital interface uses a multi-channel data frame for communicating data over the multiplexed bus, said multi-channel data frame having at least two data channels, and wherein data for said first data channel is xDSL data for an xDSL modem transferred during a first time period of said multi-channel data frame, and data for a second channel is transferred during a second time period of said multi-channel data frame.

65. (Amended) The motherboard of claim 61, wherein said receive and/or transmit signal lines can also be configured to transfer asynchronous transfer mode (ATM) cells.

66. (Amended) The motherboard of claim 61, wherein said ATM cells are associated with an ATM interface that is a Utopia I and/or II interface coupled to said digital controller over the multiplexed bus.

Please add new claims 67 - 95:

67. The method of claim 17, wherein said second time period immediately follows said first time period such that the data is transmitted immediately following said operational and/or control information.

68. The method of claim 17, wherein said first time period and said second time period occur during a word clock period, said word clock period being greater or equal to four bit clock periods.

69. The method of claim 17, wherein said first number of bit clock periods corresponds to at least one bit clock period.

70. The method of claim 17, wherein the data and said operational and/or control information are multiplexed over a plurality of data lines.

71. (New) A method of transmitting data over a digital subscriber loop (DSL) based communications link between an DSL digital circuit section and an DSL analog circuit section comprising the steps of:

(a) generating an DSL bit clock signal adapted for data transmission requirements of the DSL based communications link; and

(b) transmitting DSL data over a data line between the DSL digital circuit section and the DSL analog circuit section based on said DSL bit clock signal; and

(c) transmitting DSL operational and/or control information over said data line based on said DSL bit clock signal; and

wherein said data line is time division multiplexed so that either said DSL data or said DSL operational and/or control information is transferred between the DSL digital circuit section and the DSL analog circuit section over said data line during a single bit clock signal period.

72. (New) The method of claim 71, further including a step: (d) generating a separate DSL word clock signal based on said DSL bit clock, such that a pulse of said separate DSL word clock signal is used to mark the beginning of a sample word to be transferred over the DSL based communications link.

73. (New) The method of claim 71, wherein said DSL data includes data from digital samples and/or ATM cells.

74. (New) The method of claim 71, wherein said DSL operational and/or control information relates to power management of a DSL modem.

75. (New) The method of claim 71, wherein said DSL operational and/or control information relates to an interrupt for a software routine implemented as part of the digital circuit section.

76. (New) The method of claim 71, wherein said DSL operational and/or control information includes register settings for the DSL digital circuit section and/or the DSL analog circuit section.

77. (New) The method of claim 71, wherein said DSL operational and/or control information includes oscillator, and/or amplifier and/or filter settings for the DSL analog circuit section.

78. (New) The method of claim 71, wherein said DSL operational and/or control information has a predetermined length.

79. (New) The method of claim 77, wherein said predetermined length can be varied at least between a first length in bits (Nc) and a second length in bits (2Nc).

80. (New) The method of claim 71, wherein said DSL operational and/or control information is transferred over a bus located on a computer motherboard.

81. (New) The method of claim 75, wherein said DSL digital circuit section is incorporated as part of a North Bridge and/or a South Bridge Chipset, and said DSL analog circuit section is part of a separate analog front end located on a modem riser card.

82. (New) The method of claim 71, wherein one or more embedded operations channels is effectuated in the DSL based communications link.

83. (New) A communications system incorporating an xDSL digital communications link, the communications system comprising:

(a) a digital controller for generating xDSL transmit data to be transmitted over the xDSL digital communications link to one or more separate xDSL channels; and

(b) a bit clock signal line for carrying a bit clock signal adapted for clocking said xDSL transmit data over the xDSL digital communications link; and

(c) a plurality of parallel transmit signal lines, separate from said bit clock signal line, and coupled to said digital controller for communicating said xDSL transmit data in parallel over the xDSL digital communications link to said one or more xDSL channels; and

wherein said digital controller also generates operational and/or control information that is transmitted over said xDSL digital communications link along with said xDSL transmit data, said operational and/or control information being used by the system in connection with controlling transmission of said xDSL transmit data through said one or more separate xDSL channels.

84. (New) The system of claim 83 wherein said operational and/or control information is implemented as an embedded operations channel (EOC).

85. (New) The system of claim 84 wherein said operational and/or control information is used to provide register settings and/or circuit settings for an analog front end circuit coupled to a digital subscriber loop (DSL).

86. (New) The system of claim 83 wherein all of said bandwidth in the xDSL link and said parallel transmit signal lines can be allocated to a single active channel.

87. (New) The system of claim 83 wherein said xDSL transmit data is transmitted within a data frame that includes data for M separate channels.

88. (New) The system of claim 87 wherein said data frame is clocked using a frame clock, which frame clock is provided on a frame clock signal line separate from said bit clock signal line.

89. (New) The system of claim 83 wherein said xDSL transmit data includes ATM cells.

90. (New) A method of transmitting data over a digital communications link between a digital controller and a plurality of analog CODECs supporting a plurality of respective data channels, the method comprising the steps of:

(a) generating a bit clock within a computer system bus adapted for data transmission requirements of the digital communications link;

(b) generating a separate frame signal within said computer system bus for indicating a boundary for a data frame carrying channel data for the plurality of respective data channels;

(c) communicating said channel data within said computer system bus between the digital controller and the plurality of analog CODECs based on said bit clock and said separate frame signal using time division multiplexing, such that channel data words for each of the plurality of respective data channels are clocked at different respective portions of said data frame;

wherein a communications protocol is used so that the digital communications link supports all of said plurality of respective data channels.

91. (New) The method of claim 90, wherein each of said plurality of respective data channels can have different transmit and/or receive data rates.

92. (New) The method of claim 90, wherein operational control information is embedded in each data frame for said plurality of respective data channels.

93. (New) The method of claim 92, wherein said operational control information consists of a control data word that is transmitted asynchronously.

94. (New) The method of claim 90, wherein the digital controller section is located on a system motherboard of the computer system, and the analog CODEC is located at a position which is substantially free of electronic noise from other electronic components on said motherboard which could materially affect the operation of such analog CODEC.

95. (New) The method of claim 90 wherein the digital controller section and analog CODEC are used by an xDSL modem, and the digital communications link is used to support an xDSL compatible data transmission.

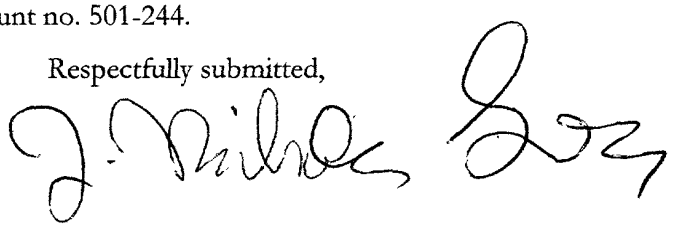
Remarks

Claims 17– 21, 27 – 31, 37 – 41 and 61 – 95 are pending. The present application is a continuation of parent application serial no. 09/255,235, which is now allowed.

The present claims are more particularly directed to those aspects of the invention that relate to communications links within a computer system that include a control channel as part of the transmission and/or which facilitate multi-channel embodiments. Support for these aspects of the invention can be found at among other places, pages 15 – 18. These inventions allow for more flexible control of broadband modem devices, including xDSL devices, multiple xDSL codecs, etc. As the prior art fails to disclose or suggest many of the claimed limitations, Applicants submit that the pending claims should be allowable at this time.

A fee transmittal sheet is enclosed; please charge any additional filing fees for the extra claims submitted herewith to deposit account no. 501-244.

Respectfully submitted,



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I hereby certify that the foregoing is being deposited with the U.S. Postal Service, postage prepaid, to the Commissioner of Patents and Trademarks, this 13th day of November, 2001.

VERSION WITH MARKINGS TO SHOW CHANGES MADE TO THE SPECIFICATION

Page 5, ll. 5 – 17:

An improved digital communications link of the present invention connects a digital controller section of an xDSL modem - which is preferably located on a system motherboard of a computing system - to a separate analog section of the xDSL modem - which is located at a position substantially free of electronic noise from other electronic components on said motherboard, which could materially affect the operation of such analog section. The data path/link is generally configured in the following manner: (a) a plurality of receive signal lines are set up for receiving data from a remote site; (b) a plurality of transmit signal lines are designated for transmitting [receiving] data to [from] a remote site; (c) a bit clock signal line is set up for carrying a clock signal, which clock signal is used in connection with communicating the data to and from the remote site. The bit clock signal line can carry any desired clock signal needed according to data transmission requirements of said digital communications link, thus providing a scalable interface that is easily adaptable for use in any number of different motherboard environments.

Page 10, lines 1 – 11:

216, which transmits signals in the DSL link to DSL Digital Modem Circuit 230, and converts received signals in the DSL link to various data and control signals for the internal circuits within DSL Analog Modem Circuit 205, including control registers 215. Also inside DSL-A 216 [218] is a clock circuit (not shown) which generates the necessary clocks for internal blocks and external DSL link based on an input from a System Master Clock as shown. Again, some or all of the functions of DSL Analog Modem Circuit 205 may be grouped and implemented in single chip form. For example, DSL-A codec 218, incorporating control registers 215, DSL-A Interface 216, digital filters 214, 214', and A/D 213 and D/A 213' is preferably embodied in a single integrated circuit (IC), and a separate IC is preferably used to embody analog front end sections (i.e. receive/transmit drivers 209, 209' and receive/transmit filters 211 and 211').

Page 11, lines 27 – 29:

As noted above, functions performed by Transmitter Buffer and Processing 234' [234] and Receiver Buffer and Processing 234 [234'] depend on the specific xDSL implementation. In the case of host signal processing, where the present invention can be used for great

Page 12, lines 24 – 26:

Receive data lines RX_1 - RX_4 carry digital samples generated by A/D 213 and assembled and transmitted across the link by DSL-A Interface 216; DSL-D interface 233, conversely dis-assembles and passes these samples on for further signal processing.

Page 18, lines 11 – 29:

--Reuse of DSL Link for External Hardware DSL Implementation

As mentioned earlier, the use of DSL Link 200 [220] is most attractive to a host based DSL modem implementation requiring minimal logic inside Digital IC 230. When the CPU in the motherboard is not fast enough, it is desirable to use the DSL Link to connect Digital IC 230 to an external hardware DSL implementation. In this case, another useful aspect of the present invention is illustrated in FIG. 4. As shown, when an external hardware solution for a DSL modem implementation exists, a reasonable interface to use with such implementation is one based on the ATM Utopia I or Utopia II interface. This is because ADSL technology has already been defined to interface with ATM in both T1.413 Issue 2 and ITU-T G.992 standards. In this configuration, DSL Digital IC 230 would be linked through DSL Digital Link 220 to a hardware based xDSL modem in FIG. 2A and 2B, instead of interfacing directly to DSL Analog Modem Circuit 205. In such instance, of course, since most of the signal processing and control functions would be located within the hardware xDSL modem, DSL Digital Controller 230 could be simplified accordingly. The reason this is possible is because the same 10 signal lines described above (RX_1 - RX_4, TX_1 - TX_4, CLOCK and WORD CLOCK) can serve a dual purpose and act as an ATM interface as well. As above, for the same four sampling cycles per word clock, the following data can be transported over DSL digital link 220:

1. First clock cycle period: RX_1 - RX_4 are used for Control, 0, RxClav, TxClav;

Page 19, lines 1 – 7:

TX_1 - TX_4 are used for Control, 0, RxEnb and TxEnb.

2. Second clock cycle period: RX_1 - RX_4 are used for RxSoc, RxAddr [2:0], while TX_1 - TX_4 are used for TxSoc, TxAddr [2:0].

3. Third clock cycle period: RX_1 - RX_4 are used for RxData [7:4] ~~[3:0]~~, while TX_1 - TX_4 are used for TxData [7:4] ~~[3:0]~~.

4. Fourth clock cycle period: RX_1 - RX_4 are used for RxData [3:0] ~~[4:7]~~, while TX_1 - TX_4 are used for TxData [3:0] ~~[4:7]~~.

VERSION WITH MARKINGS TO SHOW CHANGES TO CLAIMS

17. (Amended) A [communications protocol] method for transmitting data on an xDSL digital communications link between a digital controller and an analog codec located within a personal computer system, [said protocol] the method comprising the steps of:

(a) generating [an xDSL] a bit clock [and a separate xDSL word clock] adapted for data transmission requirements of [said analog xDSL codec] the xDSL digital communications link;

(b) communicating the data and operational and/or control information [words] between the digital controller and analog codec at a rate corresponding to said [xDSL] bit clock such that said operational and/or control information is transmitted over a data line during a first time period corresponding to a first number of bit clock periods, and the data is transmitted over said data line during a second time corresponding to a second number of bit block periods;

[(c) communicating operational and/or control information embedded] within said data words during said word clock period];

wherein both said operational and/or control information and the data can be [simultaneously] exchanged between the digital controller and the analog codec over a time division multiplexed data line.

18. (Amended) The [protocol] method of claim 17, wherein said operational and/or control information includes information relating to real time control settings for circuits located within the analog codec.

19. (Amended) The [protocol] method of claim 18, wherein said operational and/or control information further includes information relating to power management for an xDSL modem.

20. (Amended) The [protocol] method of claim 19, wherein said operational and/or control information consists of control data words that are transmitted asynchronously with respect to the data [words].

22. (Amended) The [protocol] method of claim 20, wherein said operational and/or control information consists of a control data word, and wherein a start bit is used within said operational control information to indicate the beginning of a valid control data word.

27. (Amended) A method of [communications protocol for transmitting data on an xDSL] operating a multi-channel digital communications link [between a digital controller and a plurality of analog codecs occupying a plurality of respective data channels] within a personal computer system, the method [said protocol] comprising the steps of:

(b) generating a [an xDSL] bit clock signal and a separate frame signal [xDSL word clock] adapted for data transmission requirements of [the] a plurality of separate communications channels within the personal computer system [analog xDSL codecs];

wherein said plurality of separate communications channels are supported by a communications bus coupling a digital controller and a plurality of separate communications circuits within the personal computer system;

(b) communicating data words between [the] said digital controller and [the] one or more of said plurality of [analog codecs] separate communications circuits using said bit clock signal and said separate frame signal [during said xDSL word clock];

(c) grouping [multiple] data words for one or more of said separate communications channels in a multi-channel data frame [to support the plurality of data channels] such that each of said plurality of separate communications circuits can be supported with a different transmit and/or receive data rate over said communications bus [and/or different accumulated data rates between transmit and receive directions for one or more of the plurality of analog codecs].

28. (Amended) The method [protocol] of claim 27, wherein said [word clock] frame signal is used to mark the boundary of each multi-channel data frame by having a first predetermined value for [two] a first number of bit clock cycles at the frame beginning, and said [word clock] frame signal has [said predetermined value for only one bit clock cycle for each word beginning in] a second predetermined value for the rest of [the] said multi-channel data frame.

29. (Amended) The method [protocol] of claim 27, wherein operational and/or control information for each of said plurality of [codecs] separate communications circuits is embedded in data words communicated through [the plurality of data channels] each of their respective communications channels.

30. (Amended) The method [protocol] of claim 29, wherein said operational and/or control information consists of control data words that are transmitted asynchronously with respect to data words.

31. (Amended) The method [protocol] of claim 27, wherein the digital controller section is located on a system motherboard of the computing system, and the separate communications circuits include at least one with an analog codec [is] located at a position which is substantially free of electronic noise from other electronic components on said motherboard which could materially affect the operation of such analog codec.

37. (Amended) A digital controller for use with an xDSL [capable] compatible modem comprising:

[[i]] a) means for processing xDSL formatted data [and control signals] in accordance with an xDSL transmission protocol; and

[[ii]] b) means for generating control signals associated with maintaining an xDSL compatible data link within a computer system in accordance with said xDSL transmission protocol; and

[[iii]] c) a digital interface for coupling the digital controller to an analog codec associated with [said] the xDSL compatible modem and, said digital interface being configured such that:

[i] a plurality of receive lines can be used for receiving xDSL data; and

[ii] a plurality of transmit lines can be used for transmitting xDSL data;

[iii] a bit clock signal line can be used for carrying a bit clock signal adapted for [an xDSL compatible data link] said xDSL transmission protocol; and

[iv] a [word clock] frame signal can be used for clocking xDSL data [words] in the form of an xDSL data frame transferred in parallel over said plurality of receive lines and/or said plurality of transmit lines; and

[v] [an embedded] a control channel is provided so that said control signals can be passed between said digital controller and said analog codec sections of said xDSL capable modem within at least one bit clock signal period of one or more of said xDSL data frames using said plurality of receiving lines and/or said plurality of transmitting lines; and

wherein said digital controller is adapted to be physically placed on a computer motherboard.

38. (Amended) The digital controller of claim 37, wherein said control signals are embedded within an xDSL data word and asynchronously transmitted with respect to [said] xDSL data words contained in said xDSL data frames.

39. (Amended) The digital controller of claim 37, wherein said digital interface can handle a multi-channel xDSL data frame, said multi-channel xDSL data frame having at least two data channels, and wherein data can be transferred through a first channel during a first time period of said multi-channel xDSL data frame, and through a second channel during a second time period of said multi-channel xDSL data frame.

40. (Original) The digital controller of claim 37, wherein said control signals relate to real time control settings for circuits located within the analog codec.

42. (Amended) The digital controller of claim 37, wherein said control signals relate to power management operations to be performed by [for] the xDSL capable modem.

61. (Amended) In a motherboard for use in a personal computing system, and which system is configured to support a plurality of separate communications channels using a multiplexed communication bus within the personal computing system, [treat a high speed xDSL capable modem as a motherboard device,] the improvement comprising:

(A) a digital controller controlling data transfers over the multiplexed bus [associated with the high speed modem], said digital controller being located physically on the motherboard and including:

[i] circuitry for processing [xDSL formatted] data and control signals for each of the plurality of separate communications channels; and

(B) an analog front end circuit associated with a first one of said plurality of separate communication channels[the high speed modem], said analog front end circuit being electrically coupled to the multiplexed bus but physically separated from said digital controller, said analog front end circuit including:

[i] line interface circuitry for coupling to a first data channel carrying analog data signals corresponding to [said xDSL formatted] first data transferred in accordance with a first communications standard and control signals associated with a first data transmission; and

[ii] circuitry for performing A/D and D/A operations on said analog data signals and [xDSL formatted] first data [and control] signals respectively; and

(C) a digital interface for coupling said digital controller and analog front end circuit over the multiplexed bus, said digital interface including:

[i] a plurality of [xDSL] data receiving lines; and

[ii]a plurality of [xDSL] data transmitting lines; and

[iii] a clock signal adapted for supporting transmission requirements of each of said plurality of separate communications channels [an xDSL compatible link]; and

[[iv]] wherein a plurality of separate control channels are implemented in time-multiplexed form over the multiplexed bus for each of said plurality of separate communications channels respectively [an embedded control channel data in said xDSL compatible link;]

[wherein said digital interface supports an xDSL compatible data link between said digital controller and said analog front end circuit].

62. (Amended) The motherboard of claim 61, wherein said analog front end circuit is located on a xDSL modem riser card which is configured to be mounted substantially perpendicular to the motherboard.

63. (Original) The motherboard of claim 61, wherein said digital controller is controlled in part in software by a host processor located on the motherboard.

64. (Amended) The motherboard of claim 61, further wherein said digital interface uses a multi-channel data frame for communicating data over the multiplexed bus, said multi-channel data frame having at least two data channels, and wherein data for said first data channel is xDSL data for an xDSL modem transferred [through a first channel] during a first time period of said multi-channel data frame, and data for a second channel is transferred [through a second channel] during a second time period of said multi-channel data frame.

65. (Amended) The motherboard of claim 61, wherein said receive and/or transmit signal lines can also be configured to transfer asynchronous transfer mode (ATM) cells [used to support an ATM interface for a hardware based xDSL modem].

66. (Amended) The motherboard of claim 61, wherein said ATM cells are associated with an ATM interface that is a Utopia I and/or II interface coupled to said digital controller over the multiplexed bus.